USB2813
User’s Manual

Beijing ART Technology Development Co., Ltd.

Contents

Chapter 1 Overview

In the fields of Real-time Signal Processing, Digital Image Processing and others, high-speed and high-precision data acquisition modules are demanded. ART USB2813 data acquisition module, which brings in advantages of similar products that produced in china and other countries, is convenient for use, high cost and stable performance.

ART USB2813 is a data acquisition module based on USB bus. It can be directly inserted into USB interface to constitute the laboratory, product quality testing center and systems for different areas of data acquisition, waveform analysis and processing. It may also constitute the monitoring system for industrial production process.

Unpacking Checklist

Check the shipping carton for any damage. If the shipping carton and contents are damaged, notify the local dealer or sales for a replacement. Retain the shipping carton and packing material for inspection by the dealer.
Check for the following items in the package. If there are any missing items, contact your local dealer or sales.

- USB2813 Data Acquisition Board
- ART Disk
  a) user's manual (pdf)
  b) drive
  c) catalog
- Warranty Card

FEATURES

Analog Input

- Input Range: ±10V, ±5V, 0~10V
- 12-bit resolution
- Sampling Rate: maximum 100KHz
- Analog Input Mode: 16SE/8DI
- Analog Input Impedance: >100MΩ
- System Measurement Accuracy: 0.1%
- Operating Temperature Range: 0℃~55℃
- Storage Temperature Range: -20℃~70℃
- Operational relations between amplifier gain (G)and resistance RG1: G＝1＋50KΩ/RG1

Gain	RG1(theoretical value)	proximal value（accuracy 1%）RG1
1	Null	Null
2	50.00K	49.9K
5	12.50K	12.4K
10	5.556K	5.62K
20	2.632K	2.61K
50	1.02K	1.02K
100	505.1	511
200	251.3	249

500	100.2	100
1000	50.05	49.9
2000	25.01	24.9
5000	10.00	9.88
10000	5.001	4.94

Analog Output

- Output Range: ±10V,±5V, 0~10V, 0~5V
- 12-bit resolution
- Update Rate:100KHz
- Set-up Time: 10μS (0.01%)
- Channel No.: 4-channel
- Non-linear error: ±2LSB(Maximum)
- Output Error (full-scale): ±1LSB
- Operating Temperature Range: 0℃~55℃
- Storage Temperature Range: -20℃~+70℃

Digital Input

- Channel No.: 8-channel
- Electric Standard: TTL compatible
- Maximum Absorption Current:<0.5mA
- High Voltage: ≧2V
- Low Voltage: ≦0.8V

Digital Output

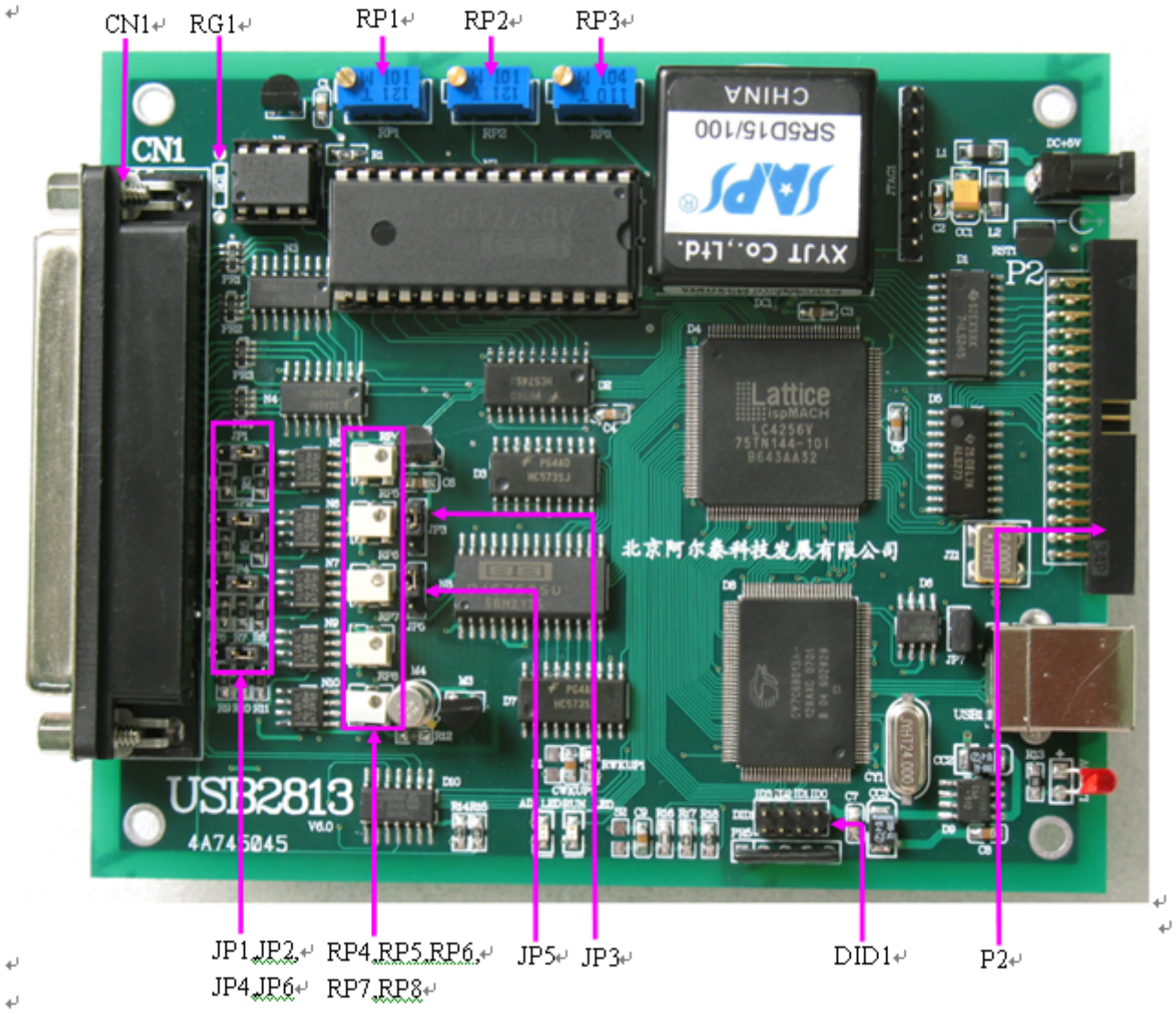
- Channel No.: 8-channel
- Electrical Standard: TTL compatible
- Maximum Pull-down Current: 20mA
- Maximum Pull-up Current: 2.6mA
- High Voltage: ≧3.4V
- Low Voltage: ≦0.5V

Counter/timer

- Counter No.: 3 separate counter
- Counter mode: subtractive counter
- 16-bit resolution
- Operate Type: 4 operate type (software-configurable)
- Counting Mode: 6 counting mode(software-configurable)
- Counting Type: binary counting and BCD code counting
- Input Electric Standard: High Level≧2.2V, Low Level≦0.8V
- Output Electric Standard: High Level≧3.0V, Low Level≦0.4V

Chapter 2 Components Layout Diagram and a Brief Description

2.1 The Main Component Layout Diagram



2.2 The Function Description for the Main Component

2.2.1 Signal Input and Output Connectors

CN1: analog signal input and output port

P2: digital signal input and output port

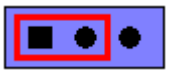
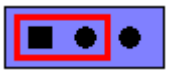
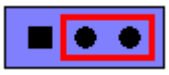
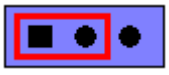
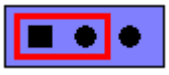
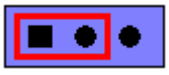
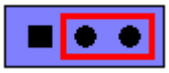
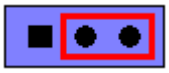
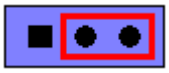
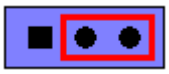
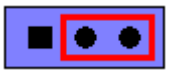
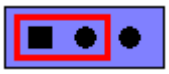
2.2.2 Potentiometer

RP1: Analog signal input full-scale adjustment potentiometer
RP2: Analog signal input bipolar zero-point adjustment potentiometer
RP3: Analog signal input unipolarity zero-point adjustment potentiometer
RP4~RP7: AO0～AO3 full-scale adjustment potentiometer
RP8: AO0～AO3 full-scale adjustment potentiometer
RG1: Amplification-related resistance

2.2.3 Jumper

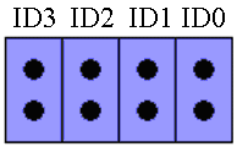
JP1, JP2, JP4, and P6: Analog signal output range selection.
JP3, JP5: Analog signal output polarity selection, unipolarity or bipolar
DID1: Physics ID Number

Analog signal output range setting

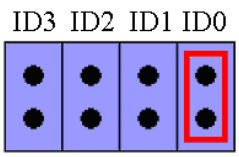
Voltage Range	JP3	JP5	JP1(AO0) JP2(AO1) JP4(AO2) JP6(AO3)
±10V			
±5V			
0～10V			
0～5V			

2.2.4 Physical ID

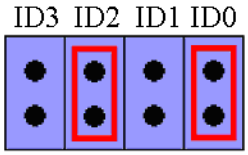
From left to right: ID3, ID2, ID1, ID0, when it is not short circuit means 0, otherwise means 1.



The above chart shows"0000", so it means that the physical ID is 0 (Binary 0000).



The above chart shows"1000", so it means that the physical ID is 1 (Binary 0001).

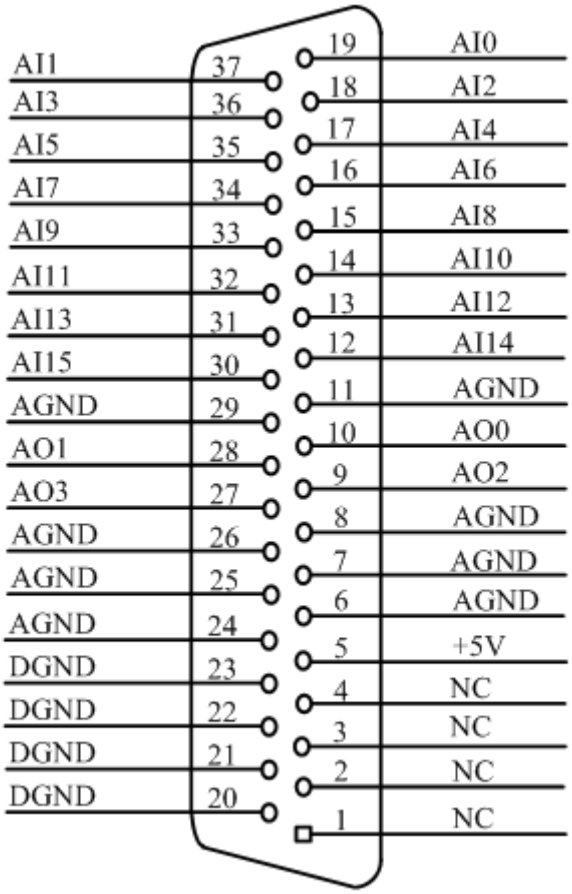


The above chart shows"1010", so it means that the physical ID is 5 (Binary0101).

Chapter 3 Signal Connectors

3.1 The Definition of Signal Input and Output Connectors

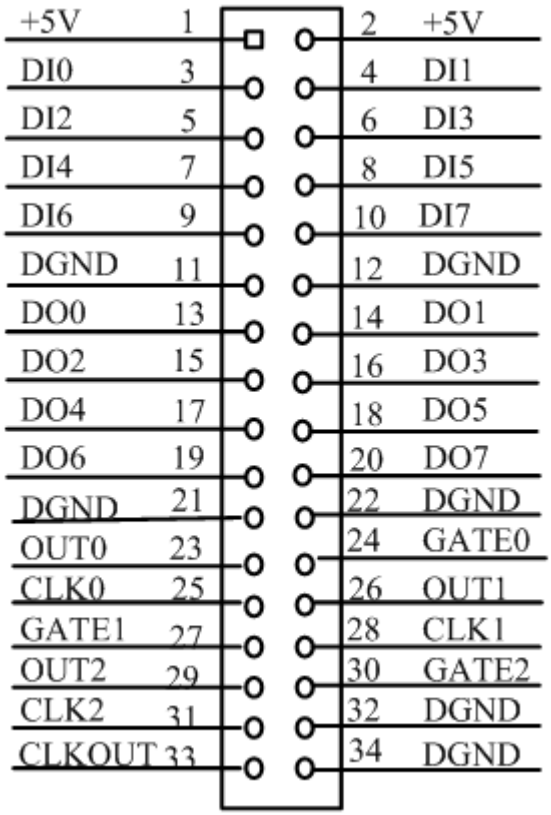
37 core plug on the CN1 pin definition



Pin definition about AD: Pin definition about AD:

Pin name	Type	Pin function definition
AI0～AI15	Input	Analog input, reference ground is AGND.
AO0～AO3	Output	Analog output.
AGND		Analog ground. This AGND pin should be connected to the system's AGND plane.
DGND		Digital ground. Ground reference for Digital circuitry. This DGND pin should be connected to the system's DGND plane.
+5V	Output	Output 5V.
NC		No connection

Pin definition about Digital Input/Output



Pin Name	Feature	Function Definition
DI0~DI7	Input	Digital signal input
DO0~DO7	Output	Digital signal output
+5V	Output	Output 5.
CLKOUT	Output	on-board 2MHz clock oscillator pulse output, Output cycle 0.5 microseconds, provides the clock source signal for CLK0~CLK2
CLK0~CLK2	Input	Clock/pulse input pins
GATE0~GATE2	Input	Gate input pins
OUT0~OUT2	Output	Output pins
DGND	GND	Digital ground, when use counter/timer we best choose it as reference ground.

Chapter 4 Connection Ways for Each Signal

4.1 Analog Input Single-ended Connection

Single-ended mode can achieve a signal input by one channel, and several signals use the common reference ground. This mode is widely applied in occasions of the small interference and relatively many channels.

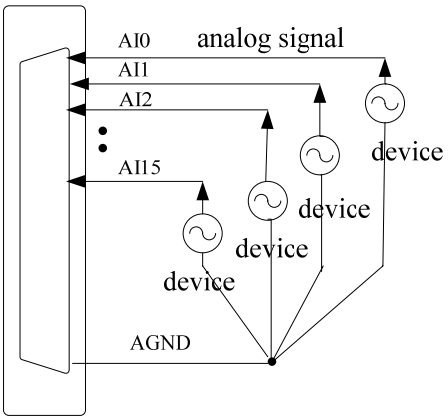


Figure 4.1 single-ended input connection

4.2 Analog Input Differential-ended Mode

Double-ended input mode, which was also called differential input mode, uses positive and negative channels to input a signal. This mode is mostly used when biggish interference happens and the channel numbers are few. Single-ended/double-ended mode can be set by the software, please refer to USB2813 software manual.

According to the diagram below, USB2813 board can be connected as analog voltage double-ended input mode, which can effectively suppress common-mode interference signal to improve the accuracy of acquisition. Positive side of the 8-channel analog input signal is connected to AI0~AI7, the negative side of the analog input signal is connected to AI8~AI15, equipments in industrial sites share the AGND with USB2813 board.

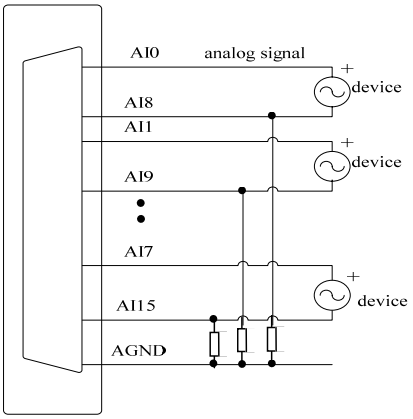


Figure 4.2 double-ended input connection

4.2 Other Connections

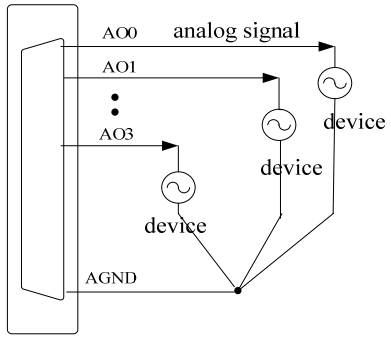


Figure 4.3 analog signal output connection

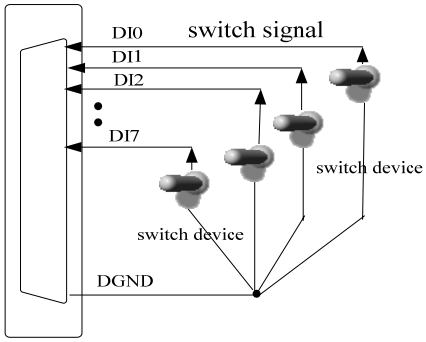


Figure 4.4 digital signal input connection

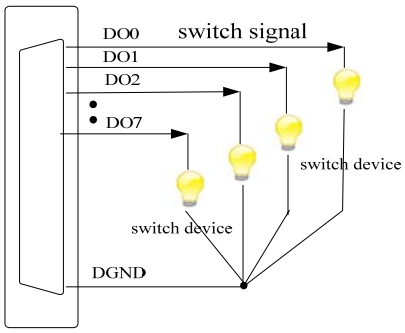


Figure 4.5 digital signal output connection

Chapter 5 Methods of using Timer/Counter 8254

5.1 The working mode

MODE 0 Interrupt on terminal count

Mode 0 is typically used for event counting. After the Control Word is written, OUT is initially low, and will remain low until the Counter reaches zero. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written into the Counter.

GATE=1 enables counting; GATE=0 disables counting. GATE has no effect on OUT.

After the Control Word and initial count are written to a Counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not go high until N+1 CLK pulses after the initial count is written.

If a new count is written to the Counter, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:
1) Writing the first byte disables counting. OUT is set low immediately (no clock pulse required)
2) Writing the second byte allows the new count to be loaded on the next CLK pulse

This allows the counting sequence to be synchronized by software. Again, OUT does not go high until N+1 CLK pulses after the new count of N is written.

If an initial count is written while GATE=0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulse later, no CLK pulse is needed to load the Counter as this has already been done.

MODE 1 Hardware retriggerable one-shot

OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and will remain low until the Counter reaches zero.
OUT will then go high and remain high until the CLK pulse after the next trigger.

After writing the Control Word and initial count, the Counter is armed. A trigger results in loading the Counter and setting OUT low on the next CLK pulse, thus starting the one-shot pulse. An initial count of N will result in a one-shot pulse N CLK cycles in duration. The one-shout is retriggerable, hence OUT will remain low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.
If a new count is written to the Counter during a one-shot pulse, the current one-shot is not affected unless the counter is retriggered. In that case, the Counter is loaded with the new count and the one-shot pulse continues until the new count expires.

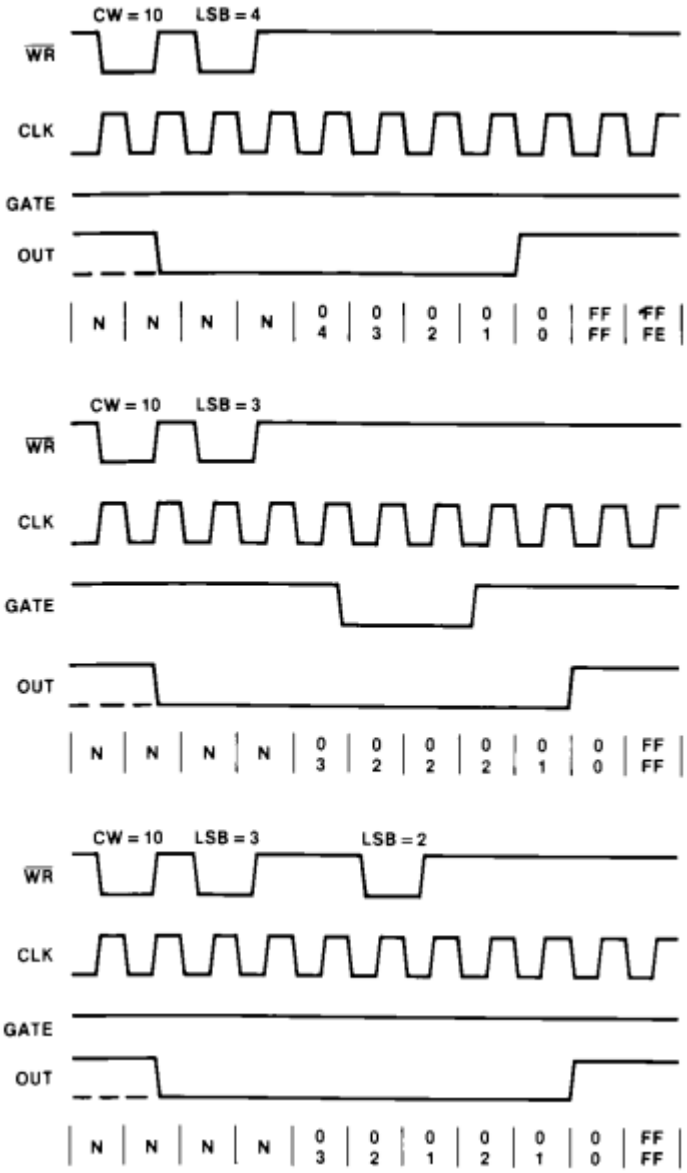


Figure 5.1 Mode 0

NOTE

The following conventions apply to all mode timing diagrams

1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant byte (LSB) only.

2. The counter is always selected ($\overline{CS}$ always low) ***错误！未指定书签。***

3. CW stands for "Control Word"; CW=10 means a control word of 10 HEX is written to the counter.

4. LSB stands for "Least Significant Byte" of count.

5. Numbers below diagrams are count values. The lower number is the least significant byte. The upper number is the most significant byte.

Since the counter is programmed to read/writer LSB only, the most significant byte cannot be read.

N stands for an undefined count.

Vertical lines show transitions between count values.

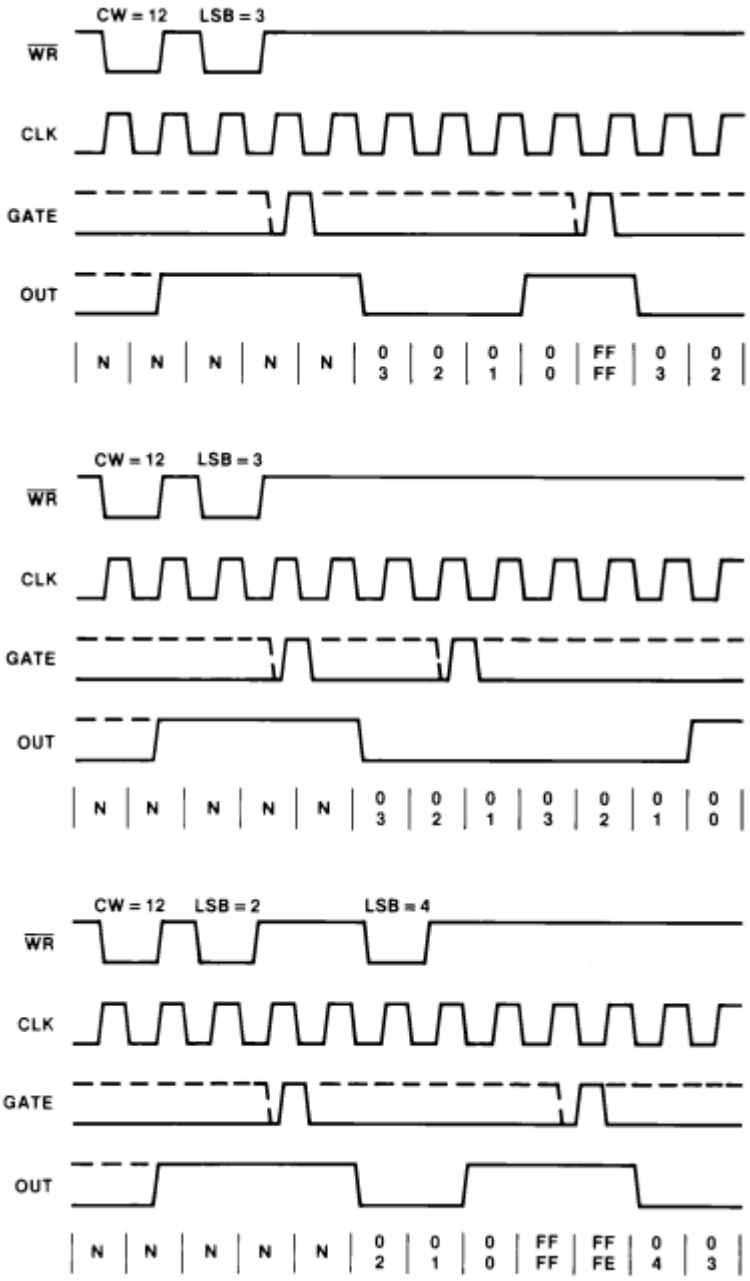


Figure 5.2 Mode 1

MODE 2 Rate Generator

This Mode functions like a divide-by-N counter. It is typically used to generate a Real Time Clock interrupt. OUT will initially be high. When the initial count has decremented to 1, OUT goes low for on CLK pulse. OUT then goes high again, the Counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.

GATE=1 enables counting; GATE=0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the Counter with the initial count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. OUT goes low N CLK Pulses after the initial count is written. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current period, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current counting cycle. In mode2, a COUNT of 1 I illegal.

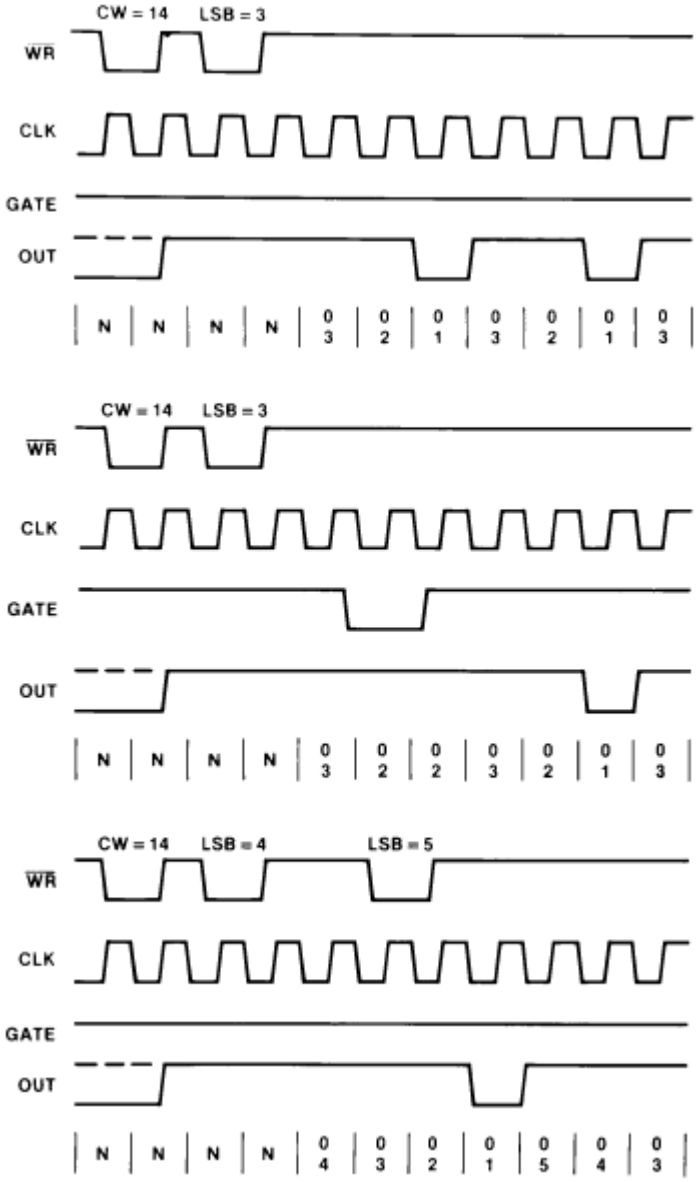


Figure 5.3 Mode 2

Note: A GATE transition should not occur one clock prior to terminal count.

MODE 3 Square wave mode

Mode 3 is typically used for Baud rate generation. Mode 3 is similar to Mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the initial count has expired, OUT goes low for mainder of the count. Mode 3 is periodic; the sequence above is repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.

GATE=1 enables counting; GATE=0 disables counting. If GATE goes low while OUT is low, OUT is set high

immediately; no CLK pulse is required. A trigger reloads the Counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the Counter

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new counter will be loaded at the end of the current half-cycle.

Mode 3 is implemented as follows:

Even counts: OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires OUT changes value and the Counter is reloaded with the initial count. The above process is repeated indefinitely.
Odd counts: OUT is initially high. The initial count minus one (an even number) is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. One CLK pulse after the count expires. OUT goes low and the Counter is reloaded with the initial count minus one. Succeeding CLK pulses decrement the count by two. When the count expires, OUT goes high again and the Counter is reloaded with the initial count minus one. The above process is repeated indefinitely. So for odd counts, OUT will be high for (N+1)/2 counts and low for (N-1)/2 counts.

MODE 4 Software triggered strobe

OUT will be initially high. When the initial count expires, OUT will go low for one CLK pulse and then go high again. The counting sequence is “triggered” by writing the initial count.

GATE=1 enables counting; GATE=0 disables counting. GATE has no effect on OUT.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N+1 CLK pulses after the initial count is written.

If a new count is written during counting, if will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:
1) Writing the first byte has no effect on counting.
2) Writing the second byte allows the new count to be loaded on the next CLK pulse.
This allows the sequence to be ‘‘retriggered’ by software. OUT strobe low N+1 CLK pulses after
the new count of N is written.

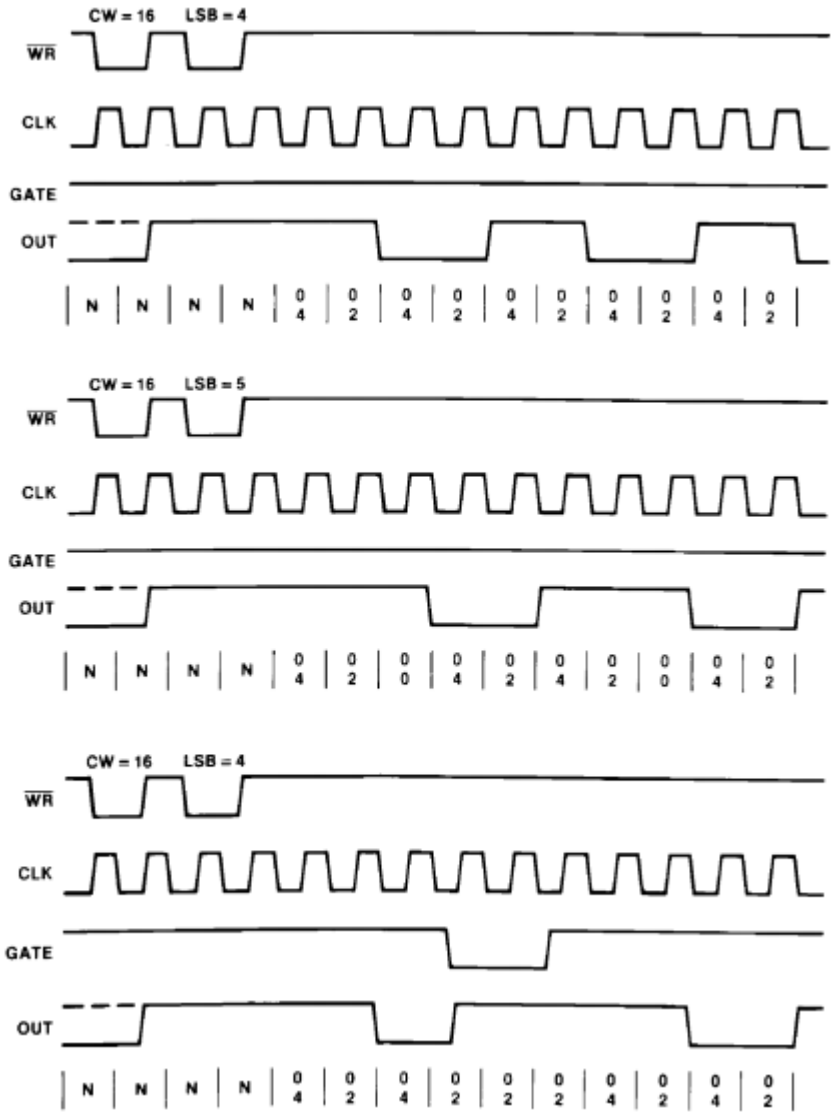


Figure 5.4 Mode 3

Note: A GATE transition should not occur one clock prior to terminal count.

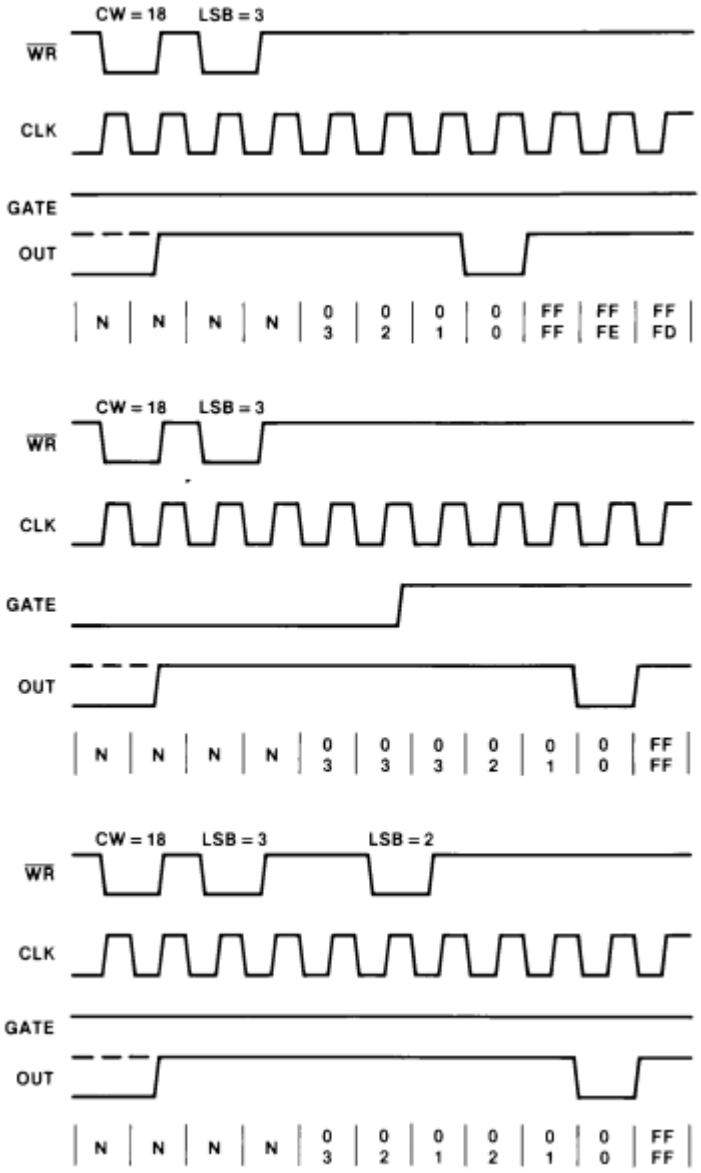


Figure 5.5 Mode 4

MODE 5 Hardware triggered strobe

OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one CLK pulse and then go high again.

After writing the Control Word and initial count, the counter will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N+ 1 pulse after a trigger.

A trigger results in the Counter being loaded with the initial count on the next CLK pulse. The counting sequence is retriggerable. OUT will not strobe low for N+1 CLK pulses after any trigger. GATE has no effect on OUT.
If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written but before the current count expires, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from there.

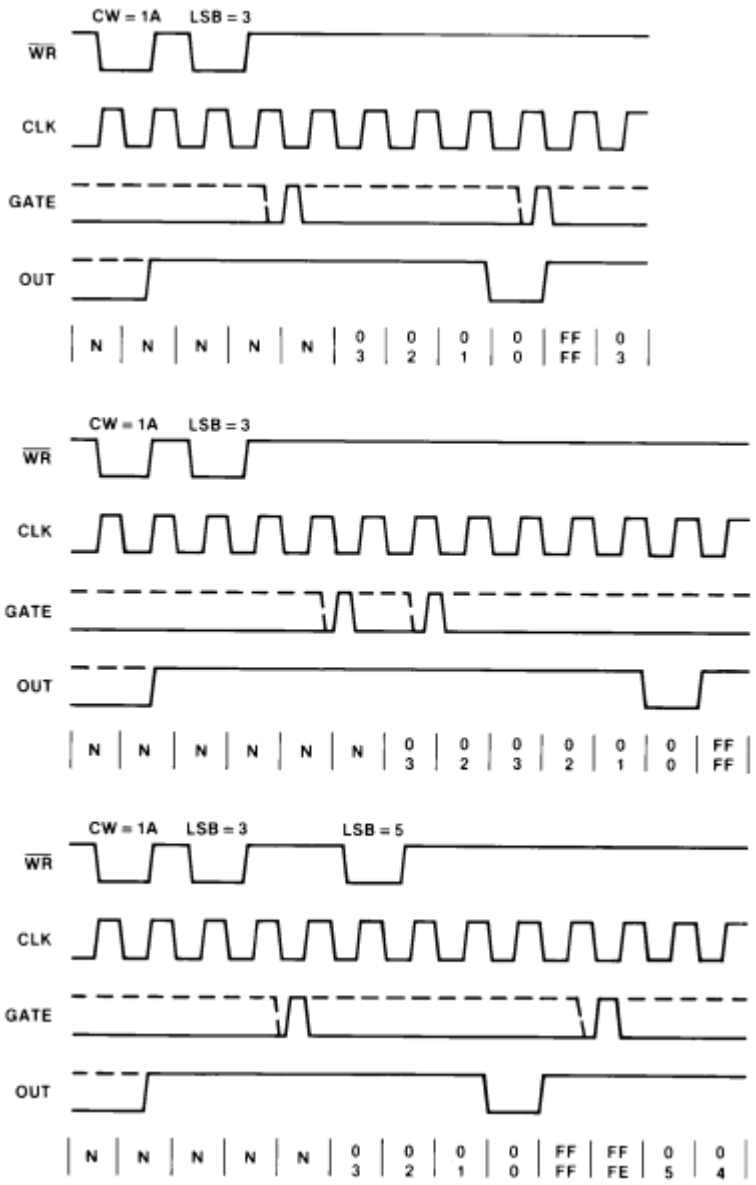


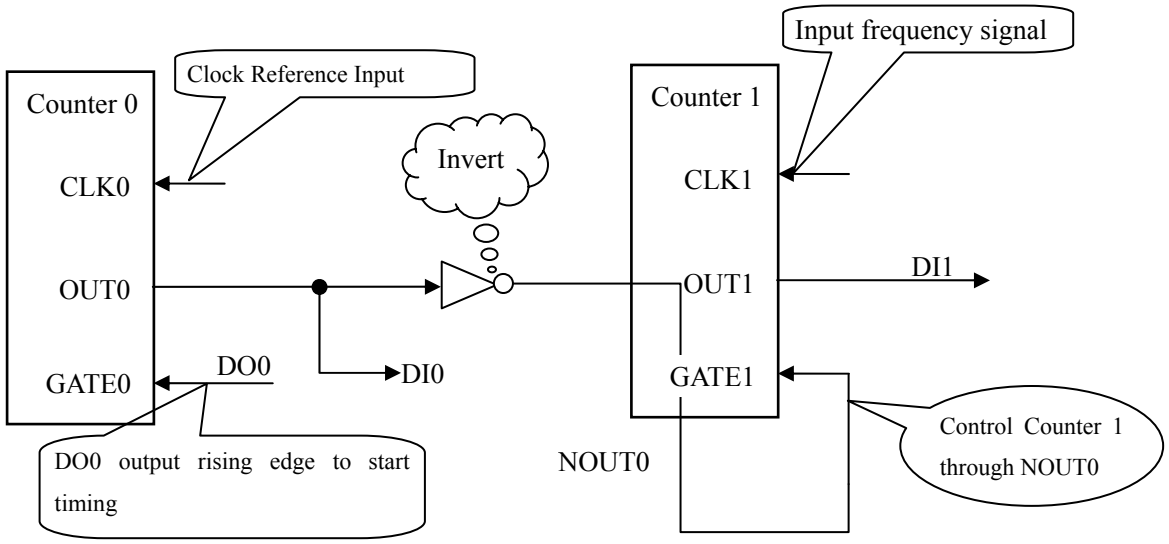
Figure5.6 Mode 5

The function of the “GATE” signal.

GATE	Low level or Falling edge	Rising edge	High level
Mode 0	Counting is forbidden	No effect	Allowed to count
Mode 1	No effect	1. Start counting after the initial value is given. 2. Re-start to counting from the initial value during one counting period.	No effect
Mode 2	Counting is forbidden and output high level	Start counting	Allowed to count
Mode 3	Counting is forbidden and output high level	Start counting	Allowed to count
Mode 4	Counting is forbidden	No effect	Allowed to count
Mode 5	No effect	1. Start counting after the initial value is given. 2. Re-start to counting from the initial value during one counting period.	No effect

Note: each timer/counter of 8254 can not set the initial value to “1” in all operating modes, for the timer/counter will stop counting and output.

5.2 Measure the frequency of an unknown frequency signal source.



Note: Counter 0 is timing channel (Mode 1), counter 1 is counting channel (Mode 0, record the number of measured signal pulse). GATE0 is controlled by DO0. Counter 0 is given an initial value which is corresponding to the time in advance. Counter is given the maximum count initial value (FFFFH). When DO0 has a rising edge, counter 0 start to timing count, its “OUT0” becomes low level; “NOUT0” becomes high level. So “GATE1” is high level, counter 1 start

to count to record the number of measured signal pulse. If counter1 counting to zero within counter 1' time, "OUT1" turns to high level. Users can read the state of DI1 to judge whether counter 1 is overflow or not. In addition, the user can read DI0 in order to judge whether the frequency measurement has completed. If DIO is high level, the frequency measurement has completed, read the value of counter 1.

At the same time it is necessary to check the state of DI1. If the state of DI1 is low level, the measured frequency is valid. If the state of DI1 is high level, the measured frequency is invalid, and re-measurement is needed. If DO0 has another rising edge, new measure can be re-started.

Chapter 6 Notes, Calibration and Warranty Policy

6.1 Notes

In our products' packing, user can find a user manual, a USB2813 module and a quality guarantee card. Users must keep quality guarantee card carefully, if the products have some problems and need repairing, please send products together with quality guarantee card to ART, we will provide good after-sale service and solve the problem as quickly as we can.

When using USB2813, in order to prevent the IC (chip) from electrostatic harm, please do not touch IC (chip) in the front panel of USB2813 module.

6.2 Analog Signal Input Calibration

Every device has to be calibrated before sending from the factory. It is necessary to calibrate the module again if users want to after using for a period of time or changing the input range. USB2813 default input range: ±10V, in the manual, we introduce how to calibrate USB2813 in ±10V, calibrations of other input ranges are similar.

Prepare a digital voltage instrument which the resolution is more than 5.5 bit, install the USB2813 module, and then power on, warm-up for fifteen minutes.

1) Zero adjustment: select one channel of analog inputs, take the channel AI0for example, connect 0V to AI0, and then run ART Data Acquisition Measurement Suite in the WINDOWS. Choose channel 0, ±10V input range and start sampling, adjust potentiometer RP2 in order to make voltage value is 0.000V or about 0.000V. Zero adjustment of other channels is alike.
2) Full-scale adjustment: select one channel of analog inputs, take the channel AI0 for example, connect 9995.12mV to AI0, and then run ART Data Acquisition Measurement Suite in the WINDOWS. Choose channel 0, ±10V input range and start sampling, adjust potentiometer RP1 in order to make voltage value is 9995.12mV or about 9995.12mV. Full-scale adjustment of other channels is alike.
3) Repeat steps above until meet the requirement.

6.3 Analog Signal Output Calibration

In the manual, we introduce how to calibrate USB2813 in ±10V output range; calibrations of other input ranges are similar.

1）Connect the ground of the digital voltage meter to any analog AGND of the CN1 37 core D-type plug. Connect the input side of the voltage meter to the DA which needs calibration. Run USB2813 test procedure under Windows, select the analog output detection.

2) Set the analog output value to 2048, adjust potentiometer RP8 in order to make output to 0.000V.

3）Set the analog output value to 4095, adjust potentiometer RP4 in order to make AO0 output value to 9995.12mV.

4）Repeat steps above until meet the requirement.

6.4 Warranty Policy

Thank you for choosing ART. To understand your rights and enjoy all the after-sales services we offer, please read the following carefully.

1. Before using ART's products please read the user manual and follow the instructions exactly. When sending in damaged products for repair, please attach an RMA application form which can be downloaded from: www.art-control.com.

2. All ART products come with a limited two-year warranty:

- The warranty period starts on the day the product is shipped from ART's factory
- For products containing storage devices (hard drives, flash cards, etc.), please back up your data before sending them for repair. ART is not responsible for any loss of data.
- Please ensure the use of properly licensed software with our systems. ART does not condone the use of pirated software and will not service systems using such software. ART will not be held legally responsible for products shipped with unlicensed software installed by the user.

3. Our repair service is not covered by ART's guarantee in the following situations:

- Damage caused by not following instructions in the User's Manual.
- Damage caused by carelessness on the user's part during product transportation.
- Damage caused by unsuitable storage environments (i.e. high temperatures, high humidity, or volatile chemicals).
- Damage from improper repair by unauthorized ART technicians.
- Products with altered and/or damaged serial numbers are not entitled to our service.

4. Customers are responsible for shipping costs to transport damaged products to our company or sales office.

5. To ensure the speed and quality of product repair, please download an RMA application form from our company website.

Products Rapid Installation and Self-check

Rapid Installation

Product-driven procedure is the operating system adaptive installation mode. After inserting the disc, you can select the appropriate board type on the pop-up interface, click the button【driver installation】; or select CD-ROM drive in Resource Explorer, locate the product catalog and enter into the APP folder, and implement Setup.exe file. After the installation, pop-up CD-ROM, shut off your computer, insert the USB card. If it is a USB product, it can be directly inserted into the device. When the system prompts that it finds a new hardware, you do not specify a drive path, the operating system can automatically look up it from the system directory, and then you can complete the installation.

Self-check

At this moment, there should be installation information of the installed device in the Device Manager (when the device does not work, you can check this item.). Open "Start -> Programs -> ART Demonstration Monitoring and Control System -> Corresponding Board -> Advanced Testing Presentation System", the program is a standard testing procedure. Based on the specification of Pin definition, connect the signal acquisition data and test whether AD is normal or not. Connect the input pins to the corresponding output pins and use the testing procedure to test whether the switch is normal or not.

Delete Wrong Installation

When you select the wrong drive, or viruses lead to driver error, you can carry out the following operations: In Resource Explorer, open CD-ROM drive, run Others-> SUPPORT-> USB.bat procedures, and delete the hardware information that relevant to our boards, and then carry out the process of section I all over again, we can complete the new installation.